WHAT IS CLAIMED IS

1. A method of converting a first data path carrying P packets per processing cycle to a second data path carrying N packets per processing cycle, wherein $N < P$, comprising:

receiving the P packets during a first processing cycle on the first data path;

storing the P packets in a queue;

shifting first data from the queue into a shift register;

selectively retrieving data from the shift register until a first set of Q packets of the P packets is retrieved; and

sending the set of Q packets on the second data path during the first processing cycle.

2. The method of claim 1, further comprising:

shifting second data from the queue into the shift register;

selectively retrieving data from the shift register until a second set of Q packets of the P packets is retrieved; and

sending the second set of Q packets on the second data path during a second processing cycle.

3. The method of claim 1, wherein the queue comprises a first-in-first-out (FIFO) queue.

4. The method of claim 1, wherein the data from the shift register is selectively retrieved based on a determination of whether the data comprises at least one of an end-of-packet indicator, a data field, and a start-of-packet indicator.

5. The method of claim 1, wherein the second path is coupled to a processing device configured to process a maximum of Q packets per processing cycle.

6. The method of claim 5, wherein the processing device comprises a Cyclical Redundancy Checker (CRC).

7. A packet processing system, comprising:

a first data path configured to receive P packets during a first processing cycle;

a queue configured to stored the P received packets;

a shift register; and

a control unit configured to:

shift data of the P packets from the queue into the shift register,

selectively retrieve data from the shift register until a first set of Q packets is retrieved, wherein $Q < P$, and

send the first set of Q packets on a second data path during the first processing cycle.

8. A method of converting a first data path carrying P packets per processing cycle to a second data path carrying Q packets per processing cycle, wherein $Q < P$, comprising:

receiving the P packets during a first processing cycle on the first data path;

storing the P packets in a queue;

shifting first data of the P packets from the queue into a shift register;

determining whether the data in the shift register comprises at least one of an end-of-packet indicator, a data field, and a start-of-packet indicator; and

sending, based on the determination, a first set of Q packets on a second data path during the first processing cycle.

9. The method of claim 8, further comprising:

shifting second data of the P packets from the queue into the shift register;

determining whether the data in the shift register comprises at least one of an end-of-packet indicator, a data field, and a start-of-packet indicator; and

sending, based on the determination, a second set of Q packets on the second data path during a second processing cycle.

10. The method of claim 8, wherein the queue comprises a first-in-first-out (FIFO) queue.

11. The method of claim 8, wherein the second data path is coupled to a processing device configured to process only Q packets per processing cycle.

12. The method of claim 11, wherein the processing device comprises a Cyclical Redundancy Checker (CRC).

13. A packet processing system, comprising:

a first data path configured to receive P packets during a first processing cycle;

a queue configured to store the P packets;

a shift register; and

a control unit configured to:

shift data from the queue into the shift register,

determine whether the data in the shift register comprises at least one of an end-of-packet indicator, a data field, and a start-of-packet indicator, and

send, based on the determination, a first set of Q packets on a second data path during the first processing cycle, wherein $Q < P$.

14. A method of processing packets, comprising:

receiving a plurality of packets on a first data path;

converting the plurality of packets on the first data path to a first packet on the second data path;

processing the first packet on the second data path during a first processing cycle;

converting the plurality of packets on the first data path to a second packet on the second data path; and

processing the second packet on the second data path during a second processing cycle.

15. The method of claim 14, wherein converting the plurality of packets on the first data path to a first packet on the second data path further comprises:

shifting a first quantity of data of the plurality of packets into a shift register;

selectively retrieving data from the shift register until the first packet is retrieved; and

sending the first packet on the first data path during the first processing cycle.

16. The method of claim 15, wherein converting the plurality of packets on the first data path to a second packet on the second data path further comprises:

shifting a second quantity of data of the plurality of packets into a shift register;

selectively retrieving data from the shift register until the second packet is retrieved; and

sending the second packet on the second data path during the first processing cycle.

17. The method of claim 15, wherein the data from the shift register is selectively retrieved based on a determination of whether the data comprises at least one of an end-of-packet indicator, a data field, and a start-of-packet indicator.

18. The method of claim 14, wherein a processing device that is configured to process only one packet per processing cycle processes the first packet on the second data path during the first processing cycle.

19. The method of claim 18, wherein the processing device processes the second packet on the second data path during the second processing cycle.

20. The method of claim 18, wherein the processing device comprises a Cyclical Redundancy Checker (CRC).

21. A packet processing system, comprising:

a first data path configured to receive P packets;

a second data path configured to carry Q packets during a first processing cycle, wherein $Q < P$;

a processing unit configured to:

convert the received P packets on the first data path to a first set of Q packets on the second data path during the first processing cycle,

convert the received P packets on the first data path to a second set of Q packets on the second data path during a second processing cycle; and

a first processing device configured to:

process the first set of Q packets on the second data path during the first processing cycle, and

process the second set of Q packets on the second data path during the second processing cycle.

22. A method of processing a plurality of packets using a single packet per cycle processing device, comprising:

receiving the plurality of packets during a first processing cycle;

storing the plurality of packets in a queue;

shifting a first quantity of data of the plurality of packets from the queue into a shift register;

selectively retrieving data from the shift register until a first packet of the plurality of packets is retrieved; and

processing the retrieved first packet during the first processing cycle.

23. The method of claim 22, further comprising:

selectively retrieving data from the shift register until a second packet of the plurality of packets is retrieved; and

processing the retrieved second packet during a second processing cycle.

24. The method of claim 22, wherein the queue comprises a first-in-first-out (FIFO) queue.

25. The method of claim 22, wherein the data from the shift register is selectively retrieved based on a determination of whether the data comprises at least one of an end-of-packet indicator, a data field, and a start-of-packet indicator.

26. The method of claim 22, wherein a processing device that is configured to process only one packet per processing cycle processes the first packet during the first processing cycle.

27. The method of claim 26, wherein a processing device that is configured to process only one packet per processing cycle processes the second packet during the second processing cycle.

28. The method of claim 26, wherein the processing device comprises a Cyclical Redundancy Checker (CRC).

29. A packet processing system, comprising:

a first data path configured to receive a plurality of packets during a first processing cycle;

a queue configured to store the plurality of packets;

a control unit configured to:

shift a first quantity of data of the plurality of packets from the queue into a shift register, and

selectively retrieve data from the shift register until a first packet of the plurality of packets is retrieved; and

a packet processing device configured to process the retrieved first packet during the first processing cycle.